What is Claimed is:

1. In a semiconductor memory device comprising a plurality of CMOS SRAM cells, being arranged on a semiconductor substrate in a matrix shape, each comprising a pair of access transistors, a pair of drive transistors, and a pair of load transistors, each region being a cell region with an elongated shape in a row direction, wherein three well regions are formed side by side in a row direction so that a second conductivity type well region may be disposed between two first conductivity type well regions on said semiconductor substrate, and wherein one of said access transistors and one of said drive transistors are formed in each of two said first conductivity type well regions within said cell region, and a pair of said load transistors is formed in said second conductivity type well region; and comprising a plurality of interconnection layers over transistors which configure said CMOS SRAM cell; the semiconductor memory device, comprising:

a plurality of paired bit lines, formed of one of said plurality of interconnection layers, each being extended in a column direction to be connected to said CMOS SRAM cell in the same column, and arranged in parallel in a row direction;

a plurality of high potential side power supply interconnections, formed of the same interconnection layer as that of said bit line, and each being arranged between said paired bit lines to be connected to said CMOS SRAM cell in the

same column;

a plurality of word lines, formed of said interconnection layer upper than that of said bit line by one layer, each being extended in a row direction to be connected to said CMOS SRAM cell in the same row, and arranged in parallel in a column direction; and

a low potential side power supply interconnection, formed of said interconnection layer upper than that of said word line by one layer, and connected to said CMOS SRAM cell.

2. In a semiconductor memory device comprising a plurality of CMOS SRAM cells, being arranged on a semiconductor substrate in a matrix shape, each comprising a pair of access transistors, a pair of drive transistors, and a pair of load transistors, each region being a cell region with an elongated shape in a row direction, wherein three well regions are formed side by side in a row direction so that a second conductivity type well region may be disposed between two first conductivity type well regions on said semiconductor substrate, and wherein one of said access transistors and one of said drive transistors are formed in each of two said first conductivity type well regions within said cell region, and a pair of said load transistors is formed in said second conductivity type well region; and comprising a plurality of interconnection layers over said transistors which configure said CMOS SRAM cell; the semiconductor memory device, comprising:

a plurality of word lines, formed of one of said plurality of interconnection layers, each being extended in a row direction to be connected to said CMOS SRAM cell in the same row, and arranged in parallel in a column direction;

a plurality of paired bit lines, formed of said interconnection layer upper than that of said word line by one layer, and each being extended in a column direction to be connected to said CMOS SRAM cell in the same column, and arranged in parallel in a row direction;

a plurality of high potential side power supply interconnections, formed of the same interconnection layer as that of said bit line, and each being arranged between said paired bit lines to be connected to said CMOS SRAM cell in the same column; and

a low potential side power supply interconnection, formed of said interconnection layer upper than that of said bit line by one layer, and connected to said CMOS SRAM cell.

3. In a semiconductor memory device comprising a plurality of CMOS SRAM cells, being arranged on a semiconductor substrate in a matrix shape, each comprising a pair of access transistors, a pair of drive transistors, and a pair of load transistors, each region being a cell region with an elongated shape in a row direction, wherein three well regions are formed side by side in a row direction so that a second conductivity type well region may be disposed between two first conductivity

type well regions on said semiconductor substrate, and wherein one of said access transistors and one of said drive transistors are formed in each of two said first conductivity type well regions within said cell region, and a pair of said load transistors is formed in said second conductivity type well region; and comprising a plurality of interconnection layers over transistors which configure said CMOS SRAM cell; the semiconductor memory device, comprising:

a plurality of high potential side power supply interconnections, formed of one of said plurality of interconnection layers, each being extended in a column direction to be connected to said CMOS SRAM cell in the same column, and arranged in parallel in a row direction;

a plurality of paired bit lines, formed of said interconnection layer upper than that of said high potential side power supply interconnection by one layer, each being extended in a column direction to be connected to said CMOS SRAM cell in the same column, and arranged in parallel in a row direction;

a plurality of word lines, formed of said interconnection layer upper than that of said bit line by one layer, each being extended in a row direction to be connected to said CMOS SRAM cell in the same row, and arranged in parallel in a column direction; and

a low potential side power supply interconnection, formed

of said interconnection layer upper than that of said word line by one layer, and connected to said CMOS SRAM cell.

4. In semiconductor memory device comprising a plurality of CMOS SRAM cells, being arranged on a semiconductor substrate in a matrix shape, each comprising a pair of access transistors, a pair of drive transistors, and a pair of load transistors, each region being a cell region with an elongated shape in a row direction, wherein three well regions are formed side by side in a row direction so that a second conductivity type well region may be disposed between two first conductivity type well regions on said semiconductor substrate, and wherein one of said access transistors and one of said drive transistors are formed in each of two said first conductivity type well regions within said cell region, and a pair of said load transistors is formed in said second conductivity type well region; and comprising a plurality of interconnection layers over transistors which configure said CMOS SRAM cell; the semiconductor memory device, comprising:

a plurality of paired bit lines, formed of one of said plurality of interconnection layers, each being extended in a column direction to be connected to said CMOS SRAM cell in the same column, and arranged in parallel in a row direction;

a plurality of high potential side power supply interconnections, formed of said interconnection layer upper than that of said bit line by one layer, each being extended

in a column direction to be connected to said CMOS SRAM cell in the same column, and arranged in parallel in a row direction;

a plurality of word lines, formed of said interconnection layer upper than that of said high potential side power supply interconnection by one layer, each being extended in a row direction to be connected to said CMOS SRAM cell in the same row, and arranged in parallel in a column direction; and

a low potential side power supply interconnection, formed of said interconnection layer upper than that of said word line by one layer, and connected to said CMOS SRAM cell.

5. A semiconductor memory device according to claim 1, wherein a width in a row direction of each region of said CMOS SRAM cell is not two times smaller than a width in a column direction thereof.

6. A semiconductor memory device according to claim 2, wherein a width in a row direction of each region of said CMOS SRAM cell is not two times smaller than a width in a column direction thereof.

7. A semiconductor memory device according to claim 3, wherein a width in a row direction of each region of said CMOS SRAM cell is not two times smaller than a width in a column direction thereof.

8. A semiconductor memory device according to claim 4, wherein a width in a row direction of each region of said CMOS SRAM cell is not two times smaller than a width in a column

direction thereof

9. A semiconductor memory device according to claim 3, wherein said word line is connected to said access transistor of said CMOS SRAM cell via an island-shaped pattern formed of said interconnection layer lower than that of said word line by one layer, and a connection between said word line and said island-shaped pattern is made by arranging a plurality of via sections per said island-shaped pattern.

10. A semiconductor memory device according to claim 4, wherein said word line is connected to said access transistor of said CMOS SRAM cell via said island-shaped pattern formed of said interconnection layer lower than that of said word line by one layer, and a connection between said word line and said island-shaped pattern is made by arranging a plurality of via sections per said island-shaped pattern.

11. A semiconductor memory device according to claim 1, wherein said low potential side power supply interconnection is connected to said CMOS SRAM cell via said island-shaped pattern for said low potential side power supply formed of said interconnection layer lower than that of said low potential side power supply interconnection by one layer, and a connection between said low potential side power supply interconnection and said island-shaped pattern for said low potential side power supply is made by arranging a plurality of via sections per said island-shaped pattern for said low potential side power supply.

12. A semiconductor memory device according to claim 2, wherein said low potential side power supply interconnection is connected to said CMOS SRAM cell via said island-shaped pattern for said low potential side power supply formed of said interconnection layer lower than that of said low potential side power supply interconnection by one layer, and a connection between said low potential side power supply interconnection and said island-shaped pattern for said low potential side power supply is made by arranging a plurality of via sections per said island-shaped pattern for said low potential side power supply.

13. A semiconductor memory device according to claim 3, wherein said low potential side power supply interconnection is connected to said CMOS SRAM cell via said island-shaped pattern for said low potential side power supply formed of said interconnection layer lower than that of said low potential side power supply interconnection by one layer, and a connection between said low potential side power supply interconnection and said island-shaped pattern for said low potential side power supply is made by arranging a plurality of via sections per said island-shaped pattern for said low potential side power supply.

14. A semiconductor memory device according to claim 4, wherein said low potential side power supply interconnection is connected to said CMOS SRAM cell via said island-shaped pattern for said low potential side power supply formed of said interconnection layer lower than that of said low potential side

power supply interconnection by one layer, and a connection between said low potential side power supply interconnection and said island-shaped pattern for said low potential side power supply is made by arranging a plurality of via sections per said island-shaped pattern for said low potential side power supply.

15. A semiconductor memory device according to claim 1, wherein said low potential side power supply interconnection is connected to said CMOS SRAM cell via said island-shaped pattern for said low potential side power supply formed of the same interconnection layer as that of the word line, and in order to make a spacing between said island-shaped pattern for said low potential side power supply and said word line large in width, or in order to make a line width of said word line wide, said word line is bent.

16. A semiconductor memory device according to claim 2, wherein said low potential side power supply interconnection is connected to said CMOS SRAM cell via said island-shaped pattern for said low potential side power supply formed of the same interconnection layer as that of the word line, and in order to make a spacing between said island-shaped pattern for said low potential side power supply and said word line large in width, or in order to make a line width of said word line wide, said word line is bent.

17. A semiconductor memory device according to claim 3, wherein said low potential side power supply interconnection

is connected to said CMOS SRAM cell via said island-shaped pattern for said low potential side power supply formed of the same interconnection layer as that of said word line, and in order to make a spacing between said island-shaped pattern for said low potential side power supply and said word line large in width, or in order to make a line width of said word line wide, said word line is bent.

18. A semiconductor memory device according to claim 4, wherein said low potential side power supply interconnection is connected to said CMOS SRAM cell via said island-shaped pattern for said low potential side power supply formed of the same interconnection layer as that of said word line, and in order to make a spacing between said island-shaped pattern for said low potential side power supply and said word line large in width, or in order to make a line width of said word line wide, said word line is bent.

19. A semiconductor memory device according to claim 1, wherein a plurality of low potential side power supply interconnections are arranged in parallel in a row direction, and are arranged so as to cover the bit line.

20. A semiconductor memory device according to claim 2, wherein a plurality of low potential side power supply interconnections are arranged in parallel in a row direction, and are arranged so as to cover the bit line.

21. A semiconductor memory device according to claim 3,

wherein a plurality of low potential side power supply interconnections are arranged in parallel in a row direction, and are arranged so as to cover the bit line.

22. A semiconductor memory device according to claim 4, wherein a plurality of low potential side power supply interconnections are arranged in parallel in a row direction, and are arranged so as to cover the bit line.

23. A semiconductor memory device according to claim 1, wherein there is provided a high potential side power supply reinforcement interconnection which is formed of the same interconnection as that of the low potential side power supply interconnection, and is connected to the high potential side power supply interconnection.

24. A semiconductor memory device according to claim 2, wherein there is provided a high potential side power supply reinforcement interconnection which is formed of the same interconnection as that of the low potential side power supply interconnection, and is connected to the high potential side power supply interconnection.

25. A semiconductor memory device according to claim 3, wherein there is provided a high potential side power supply reinforcement interconnection which is formed of the same interconnection as that of the low potential side power supply interconnection, and is connected to the high potential side power supply interconnection.

26. A semiconductor memory device according to claim 4, wherein there is provided a high potential side power supply reinforcement interconnection which is formed of the same interconnection as that of the low potential side power supply interconnection, and is connected to the high potential side power supply interconnection.

27. A semiconductor memory device according to claim 23, wherein a connection between the high potential side power supply reinforcement interconnection and the high potential side power supply interconnection is made in a substrate contact cell region for ensuring a substrate potential of a transistor which configures the CMOS SRAM cell.

28. A semiconductor memory device according to claim 24, wherein a connection between the high potential side power supply reinforcement interconnection and the high potential side power supply interconnection is made in a substrate contact cell region for ensuring a substrate potential of a transistor which configures the CMOS SRAM cell.

29. A semiconductor memory device according to claim 25, wherein a connection between the high potential side power supply reinforcement interconnection and the high potential side power supply interconnection is made in a substrate contact cell region for ensuring a substrate potential of a transistor which configures the CMOS SRAM cell.

30. A semiconductor memory device according to claim 26,

wherein a connection between the high potential side power supply reinforcement interconnection and the high potential side power supply interconnection is made in a substrate contact cell region for ensuring a substrate potential of a transistor which configures the CMOS SRAM cell.

31. A semiconductor memory device according to claim 1, wherein the semiconductor memory device provides a power supply reinforcement interconnection which is formed of the same interconnection layer as that of the word line within a substrate contact cell region for ensuring a substrate potential of a transistor which configures the CMOS SRAM cell, and is extended in a row direction; and connects said power supply reinforcement interconnection to said high potential side power supply interconnection or said low potential side power supply interconnection in an intersection point to the high potential side power supply interconnection or the low potential side power supply interconnection.

32. A semiconductor memory device according to claim 2, wherein the semiconductor memory device provides a power supply reinforcement interconnection which is formed of the same interconnection layer as that of the word line within a substrate contact cell region for ensuring a substrate potential of a transistor which configures the CMOS SRAM cell, and is extended in a row direction; and connects said power supply reinforcement interconnection to said high potential

side power supply interconnection or said low potential side power supply interconnection in an intersection point to the high potential side power supply interconnection or the low potential side power supply interconnection.

33. A semiconductor memory device according to claim 3, wherein the semiconductor memory device provides a power supply reinforcement interconnection which is formed of the same interconnection layer as that of the word line within a substrate contact cell region for ensuring a substrate potential of a transistor which configures the CMOS SRAM cell, and is extended in a row direction; and connects said power supply reinforcement interconnection to said high potential side power supply interconnection or said low potential side power supply interconnection in an intersection point to the high potential side power supply interconnection or the low potential side power supply interconnection.

34. A semiconductor memory device according to claim 4, wherein the semiconductor memory device provides a power supply reinforcement interconnection which is formed of the same interconnection layer as that of the word line within a substrate contact cell region for ensuring a substrate potential of a transistor which configures the CMOS SRAM cell, and is extended in a row direction; and connects said power supply reinforcement interconnection to said high potential side power supply interconnection or said low potential side

power supply interconnection in an intersection point to the high potential side power supply interconnection or the low potential side power supply interconnection.

35. A semiconductor memory device according to claim 1, wherein the low potential side power supply interconnection is formed into a mesh shape.

36. A semiconductor memory device according to claim 2, wherein the low potential side power supply interconnection is formed into a mesh shape.

37. A semiconductor memory device according to claim 3, wherein the low potential side power supply interconnection is formed into a mesh shape.

38. A semiconductor memory device according to claim 4, wherein the low potential side power supply interconnection is formed into a mesh shape.

39. A semiconductor memory device according to claim 3, wherein a film thickness of an interconnection layer forming the word line is made thicker than a film thickness of an interconnection layer lower than the word line.

40. A semiconductor memory device according to claim 4, wherein a film thickness of an interconnection layer forming the word line is made thicker than a film thickness of an interconnection layer lower than the word line.

41. A semiconductor memory device according to claim 1, wherein a film thickness of an interconnection layer forming

the low potential side power supply interconnection is made thicker than a film thickness of an interconnection lower than said low potential side power supply interconnection.

42. A semiconductor memory device according to claim 2, wherein a film thickness of an interconnection layer forming the low potential side power supply interconnection is made thicker than a film thickness of an interconnection lower than said low potential side power supply interconnection.

43. A semiconductor memory device according to claim 3, wherein a film thickness of an interconnection layer forming the low potential side power supply interconnection is made thicker than a film thickness of an interconnection lower than said low potential side power supply interconnection.

44. A semiconductor memory device according to claim 4, wherein a film thickness of an interconnection layer forming the low potential side power supply interconnection is made thicker than a film thickness of an interconnection lower than said low potential side power supply interconnection.

45. A semiconductor memory device according to claim 1, wherein the semiconductor memory device does not have a row redundant circuit but has only a column redundant circuit as a redundant circuit.

46. A semiconductor memory device according to claim 2, wherein the semiconductor memory device does not have a column redundant circuit but has only a row redundant circuit as a

redundant circuit.